ANALOG DEVICES

Key Sheet
AD7193

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Highlights of the AD7193 Low Noise, 24-Bit Sigma-Delta ADC

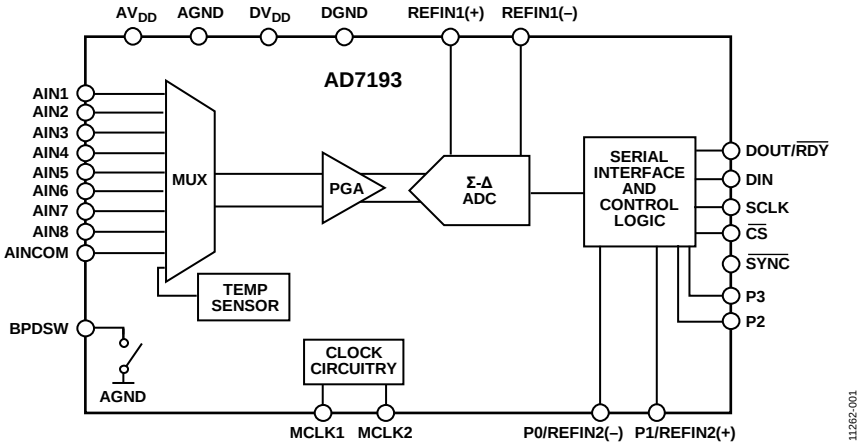

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

This key sheet[1] provides users with an overview of the AD7193. Key attributes of the part include the following:

- Designed for the measurement of wide dynamic range, low frequency signals, such as those in pressure transducers, strain gauge transducers, flow measurement, chromatography, and data acquisition systems.
- Low power, flexible, high performance, ultralow noise, 24-bit Sigma-Delta (Σ-Δ) ADC suitable for converting low input bandwidth analog signals with a fully flexible output data rate (ODR) between 4.7 SPS to 4.8 kSPS.
- An on-chip low noise gain stage allows signals of small amplitude to interface directly to the ADC.
- Combines four differential or eight pseudo differential input channels with low power consumption.
- With an ODR of 4.7 SPS and a gain of 128, the AD7193 boasts an rms noise of 11 nV.
- User friendly, with the part being fully configurable over a 4-wire serial interface.
- Available in 28-lead TSSOP and 32-lead LFCSP packages.

FEATURES AND BENEFITS

The AD7193 offers the following features and benefits:

- Mains power supply interference
- Simultaneous 50 Hz and 60 Hz rejection at 50 SPS ODR
- Programmable gains of 1, 8, 16, 32, 64, and 128
- Automatic channel sequencer
- On-chip temperature sensor
- Internal and system calibration on chip
- Option of 4.92 MHz internal clock or external crystal
- Digital filter options include using a Sinc^4 or Sinc^3 filter, chop enabled or disabled, fast settling, and zero latency
- Ultralow noise performance across the ODR range
- Fully SPI, QSPI™, MICROWIRE®, and DSP compatible
- SPI configuration control
- 3-wire serial digital interface (Schmitt trigger on SCLK)

[1] This document provides users with an overview of the AD7193; it is not a notice of performance or intent. Refer to the AD7193 data sheet for performance and more specific information about this product.

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KEY CHARACTERISTICS

FUNDAMENTAL SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit
ADC Type		Σ- Δ ADC		
Number of Input Channels		Four differential or eight pseudo differential input channels		
Resolution	24		24	Bits
Output Data Rate	4.7		4800	SPS
Differential ADC Input Range	$-V_{REF}$/gain		$+V_{REF}$/gain	V
AV_{DD} with Respect to AGND	3		5.25	V
AI_{DD} Current				
With Gain = 1, Buffer Off		0.85	1	mA
With Gain = 16 to 128, Buffer On		4.3	5.3	mA
DI_{DD} Current (DV_{DD} = 3 V)		0.35	0.4	mA
Offset Error		±150/gain		µV/gain
Offset Error Drift vs. Temperature[1]		±150/gain		nV/°C/gain
Full-Scale Error		±10		µV
Gain Drift vs. Temperature		±1		ppm/°C
Integral Nonlinearity (INL)[2]	−10	±2	+10	ppm of FSR
Power Supply Rejection		90		dB
Operating Temperature Range	−40		+105	°C

[1] Gain = 1 to 16; chop disabled.
[2] AV_{DD} = 5 V, Gain = 1.

NOISE

Sinc⁴ Chop Disabled Filter Setting

Table 2. RMS Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	RMS Noise (nV)					
			G = 1	G = 8	G = 16	G = 32	G = 64	G = 128
1023	4.7	852.5	340	53	34	18	12	11
96	50	80	950	150	80	50	37	31
80	60	66.7	1000	160	90	54	40	35
1	4800	0.83	26,000	3400	1700	910	530	380

Fast Settling Filter Setting

Table 3. RMS Noise (nV) vs. Gain and Output Data Rate

Filter Word (Decimal)	Output Data Rate (Hz)	Settling Time (ms)	RMS Noise (nV)					
			G = 1	G = 8	G = 16	G = 32	G = 64	G = 128
96	2.63	380	380	87	52	33	15	11
30	8.4	118.75	620	140	71	43	30	21
6	42.10	23.75	1300	270	150	82	56	47
5	50.53	19.79	1500	280	160	88	61	50
2	126.32	7.92	2300	380	210	130	88	77
1	252.63	3.96	3400	520	290	180	130	110

OPERATING THE AD7193

DATA INTERFACE

The data interface for the AD7193 is

- Performed using a 4- or 3-wire SPI
- Compatible with QSPI, MICROWIRE, and DSP
- Allows a user to both write to and read from the AD7193 on the same data bus
- Indicates when transferred data is available by bringing the DOUT/$\overline{RDY}$ signal and the $\overline{RDY}$ bit in the status register low

4-Wire Serial Interface

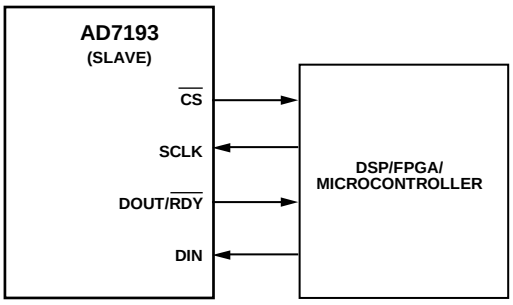


Figure 2. AD7193 Data Interface, 4-Wire SPI

Table 4. 4-Wire Serial Interface Pin Functions

Pin	Function
$\overline{CS}$	Selects the ADC (also applicable in systems with multiple devices on the serial bus).
	Provides a frame synchronization signal.[1]
SCLK	Determines when data transfers (either on DIN or DOUT/$\overline{RDY}$) occur.
DOUT/$\overline{RDY}$	Accesses data from the on-chip registers.
	Indicates when the transferred data is available.
DIN	Transfers data into the on-chip registers.

[1] Useful for DSP interfaces. The first bit (MSB) is effectively clocked out by $\overline{CS}$ because $\overline{CS}$ typically occurs after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers, provided the timing numbers are obeyed.

3-Wire Serial Interface

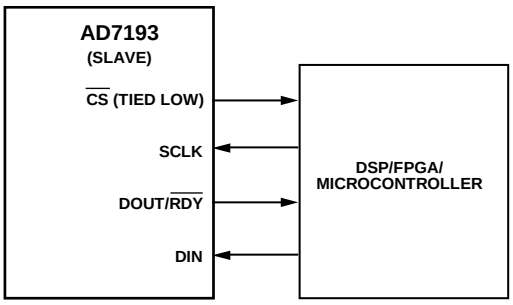


Figure 3. AD7193 Data Interface, 3-Wire SPI

Table 5. 3-Wire Serial Interface Pin Functions

Pin	Function
$\overline{CS}$	$\overline{CS}$ is permanently tied low in the 3-wire interface. (If $\overline{CS}$ is required as a decoding signal, it can be generated from a port pin.)
SCLK	Determines when data transfers (either on DIN or DOUT/$\overline{RDY}$) occur.
DOUT/$\overline{RDY}$	Accesses data from the on-chip registers.
	Indicates when the transferred data is available.
DIN	Transfers data into the on-chip registers.

DATA MODES

There are three data modes available: continuous conversion mode, continuous read mode, and single conversion mode.

Continuous Conversion Mode (Default)

Continuous conversion is the default power-up mode. In this mode, the AD7193 converts continuously, and the $\overline{RDY}$ bit in the status register goes low each time a conversion is complete. If $\overline{CS}$ is low, the DOUT/$\overline{RDY}$ line also goes low when a conversion is complete. To read a conversion, the user writes to the communications register, indicating that the next operation is a read of the data register. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. The user can read this register additional times, if required.

When several channels are enabled, the ADC continuously loops through the enabled channels, performing one conversion on each channel per loop. The data register is updated as soon as each conversion is available. The DOUT/$\overline{RDY}$ pin pulses low each time a conversion is available. The user can then read the conversion while the ADC converts on the next enabled channel.

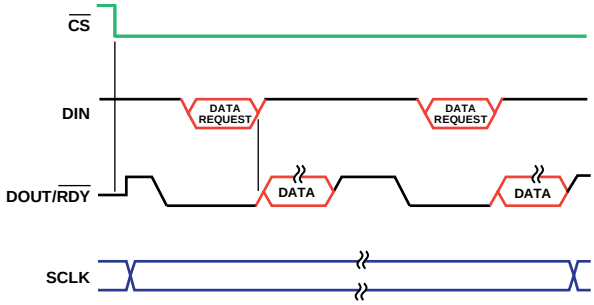


Figure 4. Continuous Conversion Mode

Continuous Read Mode

Rather than write to the communications register each time a conversion is complete to access the data, the AD7193 can be configured so that the conversions are automatically placed on the DOUT/$\overline{RDY}$ line. By writing 01011100 to the communications register, the user need only apply the appropriate number of SCLK cycles to the ADC, and the conversion word is automatically placed on the DOUT/$\overline{RDY}$ line when a conversion is complete.

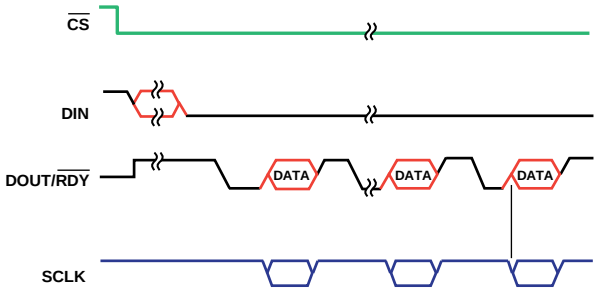


Figure 5. Continuous Read Mode

When DOUT/$\overline{RDY}$ goes low to indicate the end of a conversion, sufficient SCLK cycles must be applied to the ADC. The data conversion is then placed on the DOUT/$\overline{RDY}$ line. When the conversion is read, DOUT/$\overline{RDY}$ returns high until the next conversion is available. In this mode, the data can be read only once.

When several channels are enabled, the ADC continuously loops through the enabled channels, performing one conversion on each channel per loop. DOUT/$\overline{RDY}$ pulses low when a conversion is available. When the user applies sufficient SCLK pulses, the data is automatically placed on the DOUT/$\overline{RDY}$ pin.

Single Conversion Mode

In single conversion mode, the AD7193 performs a single conversion and is placed in standby mode after the conversion is complete. DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. The data register can be read several times, if required, even when DOUT/$\overline{RDY}$ has gone high.

If several channels are enabled, the ADC sequences through the enabled channels and performs a conversion on each channel. When a conversion is started, DOUT/$\overline{RDY}$ goes high and remains high until a valid conversion is available. As soon as a conversion is available, DOUT/$\overline{RDY}$ goes low. The ADC then selects the next channel and begins another conversion. The user can read the present conversion while the next conversion is being performed.

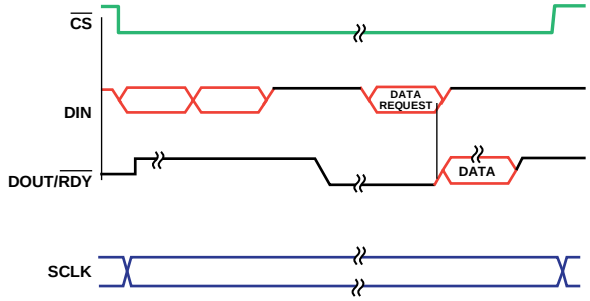


Figure 6. Single Conversion Mode

TYPICAL APPLICATION DIAGRAM

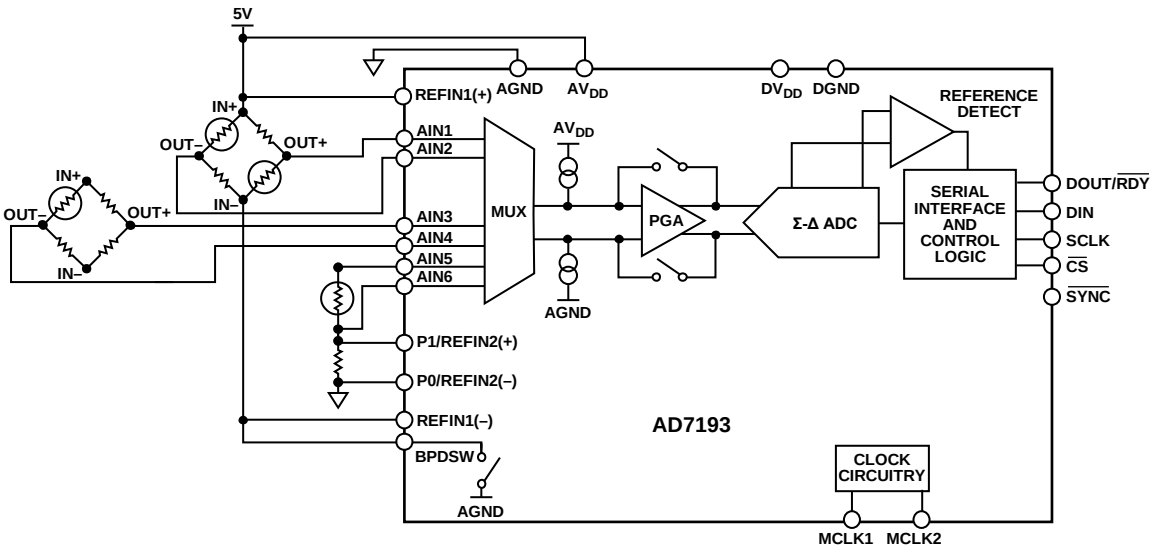


Figure 7. Typical Application Diagram

FREQUENTLY ASKED QUESTIONS

What is the optional internal buffer?
The multiplexed input channels of the AD7193 are connected to the on-chip buffer amplifier when the device is operated in buffered mode and are connected directly to the modulator when the device is operated in unbuffered mode. In buffered mode, the input channel feeds into a high impedance input stage of the buffer amplifier. Therefore, the input can tolerate significant ranges of source impedances and is tailored for direct connection to external resistive-type sensors, such as strain gauges or resistance temperature detectors (RTDs).

What digital filter options are available?
The AD7193 offers a lot of flexibility in the digital filter. The device has five filter options. The device can be operated with a $sinc^3$ or $sinc^4$ filter, chop can be enabled or disabled, and zero latency can be enabled. Finally, an averaging block can be included after the sinc filter, which allows a fast settling mode. The option selected affects the output data rate, settling time, and 50 Hz/60 Hz rejection.

What is 50 Hz and 60 Hz rejection?
The mains power supply generates interference at 50 Hz or 60 Hz, with the frequency varying from one country to another. The AD7193 has the ability to simultaneously reject 50 Hz and 60 Hz signals. The output data rate at which simultaneous 50 Hz and 60 Hz rejection occurs depends on the filter type used.

How do I interface with the part?
The part can be configured by using a 4-wire SPI interface; this interface is also used as the data interface. The SPI interface allows the user to read the status of the part and to change the setup.

Are there any ESD protection schemes that should be considered with the AD7193?
These converters are manufactured on a standard CMOS process; therefore, all standard practices and protection schemes that apply to other CMOS devices also apply to these devices. There are ESD protection diodes on all the inputs that protect the device from possible ESD damage due to handling and production. To determine the appropriate ESD precautions, refer to the AD7193 data sheet for information about the absolute maximum ratings.

Is an antialiasing filter required?
The analog input is sampled at 307.2 kHz. The digital filter does not provide any rejection at this frequency or at frequencies that are multiples of 307.2 kHz. Although an external antialiasing filter is required to provide rejection at these frequencies, a simple RC filter is sufficient. Typical values for the filter are

- 1 kΩ resistor in series with each analog input
- 0.1 µF capacitor between the analog input pins
- 0.01 µF capacitor from each input pin to ground

These typical values can be used only when the buffer is enabled. When the buffer is disabled, smaller RC values are required because larger values can cause gain errors.

Can filtering be added to the reference pins?
The reference input to the AD7193 is not buffered. Therefore, the filtering must be limited on the reference pins because large RC values can cause gain errors. The AD7193 data sheet lists acceptable RC values for use when the analog inputs are unbuffered. Similar values should be used on the reference pins.

What can the four GPIOs be used for?
The AD7193 has four general-purpose digital outputs: P0, P1, P2, and P3. The pins can be pulled high or low using the P0DAT to P3DAT bits in the GPOCON register. The logic levels for these pins are determined by AV_{DD} rather than by DV_{DD}. These pins can be used to drive external circuitry, such as an external multiplexer. If an external multiplexer is used to increase the channel count, the multiplexer logic pins can be controlled via the AD7193 general-purpose output pins. The general-purpose output pins can be used to select the active multiplexer pin.

LEARN MORE AND START DESIGNING

To learn more about the AD7193 and compatible products or to sample and buy the AD7193 device, click on the links provided or contact an Analog Devices, Inc., sales representative.

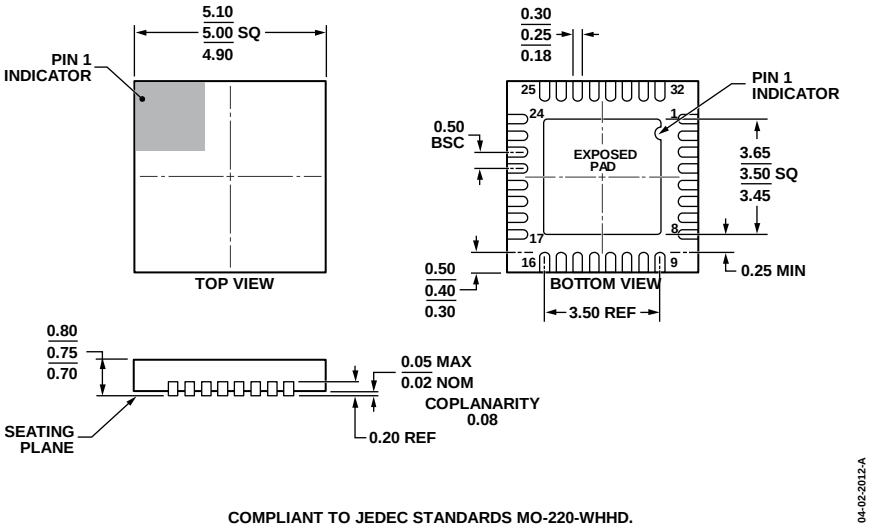
COMPATIBLE DEVICES

Table 6. Recommended Compatible Devices[1]

Linear Regulators	Precision References	ADC Driver Amplifiers	Circuits from the Lab™	Evaluation Board
ADP3303 family ADP3330 family	ADR421 family ADR431 family	N/A (the AD7193 includes an on-board internal buffer)	CN-0209, *Fully Programmable Universal Analog Front End for Process Control Applications*	AD7193 evaluation board

[1] Information about additional companion products are provided on the AD7193 product page.

PACKAGE DIAGRAM



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 8. Package Diagram

GETTING STARTED

AD7193 DATA SHEET

SAMPLE AND BUY THE AD7193